

WHAT IS CLAIMED IS:

1. A liquid crystal display (LCD), comprising:

a first gate line block including a plurality of first gate lines transmitting scanning signals, said first gate line block scanning in a first direction;

5 a second gate line block including a plurality of second gate lines transmitting scanning signals, said second gate line block scanning in a second direction;

a plurality of first data lines transmitting image signals and crossing the first gate lines of said first gate line block;

10 a plurality of second data lines transmitting image signals and crossing the second gate lines of said second gate line block; and

a plurality of pixels configured in a matrix pattern and defined by the gate lines and the data lines, said pixels including switching elements coupled to the gate lines and the data lines,

15 wherein the first direction is opposite to the second direction and the first data lines are separated from the second data lines.

2. The LCD of claim 1, wherein the number of the first gate lines is equal to the number of the second gate lines.

3. The LCD of claim 2, wherein the first gate lines and the second gate lines are simultaneously scanned.

4. A liquid crystal display (LCD), comprising:

an LCD panel including:

a first gate line block having a plurality of first gate lines;

a second gate line blockhaving a plurality of second gate lines,
said second gate line block formed beneath said first gate line block;

a plurality of first data lines crossing and separated from the first gate lines of said first gate line block;

5 a plurality of second data lines crossing and separated from the
second gate lines of said second gate line block; and

a plurality of pixels formed by areas defined by the gate lines and the data lines, and arrayed in a matrix pattern, the pixels having switching elements coupled to the gate lines and the data lines, and common electrodes to which common voltage is supplied;

a first data driver supplying data voltages, which contain image signals,
to the first data lines;

a second data driver supplying data voltages, which contain image signals, to the second data lines;

15 a first gate driver supplying scanning signals to the gate lines of said first
gate line block;

a second gate driver supplying scanning signals to the gate lines of said second gate line block in a scanning direction opposite to that of said first gate driver;

20 a first frame memory that receives and writes external image signals in
synchronization with the write clock signals and outputs the image signals to
the first data driver in synchronization with the read clock signals; and

a second frame memory that receives and writes external image signals in synchronization with the write clock signals and outputs the image signals to the second data driver in synchronization with the read clock signals.

5 Sub C1 5. The LCD of claim 4, wherein the number of the first gate lines is equal to the number of the second gate lines.

6. The LCD of claim 5, wherein said first gate driver and said second gate driver scan simultaneously.

10 7. The LCD of claim 5, wherein polarities of the data voltages supplied to the pixels coupled to adjacent gate lines of said first gate line block are opposite to each other with respect to the common voltage, and the polarities of the data voltages supplied to the pixels coupled to the neighboring gate lines of said second gate line block are opposite to each other with respect to the common voltage.

15 8. The LCD of claim 7, wherein said first gate driver sequentially supplies the scanning signals to the gate lines from the last gate line to the first gate line of said first gate line block, and said second gate driver sequentially supplies the scanning signals to the gate lines from the first gate line to the last gate line of said second gate line block.

20 Sub B3 9. The LCD of claim 8, wherein said first frame memory outputs to said first data driver the image signals in a reverse order to which the image signals are written in, and said second frame memory outputs to said second data driver in the same order as the image signals are written in.

Sub C1 10. The LCD of claim 9, wherein the polarity of the common voltage, with respect to the data voltage supplied to the pixels coupled to the last gate line of

said first gate line block, is opposite to that of the common voltage, with respect to the data voltage supplied to the pixels coupled to the first gate line of said second gate line block on the identical pixel column.

11. The LCD of claim 9, wherein the polarity of the common voltage, with respect to the data voltage supplied to the pixels coupled to the last gate line of said first gate line block, is identical to that of the common voltage, with respect to the data voltage supplied to the pixels coupled to the first gate line of said second gate line block on the identical pixel column.

12. The LCD of claim 7, wherein said first gate driver sequentially supplies the scanning signals to the gate lines from the first gate line to the last gate line of said first gate line block, and the second gate driver sequentially supplies the scanning signals to the gate lines from the last gate line to the first gate line of said second gate line block.

13. The LCD of claim 12, wherein said first frame memory outputs to said first data driver, the image signals, in the same order as the image signals are written, and said second frame memory outputs to said second data driver the image signals, which are written in a reverse order as the image signals are written.

14. The LCD of claim 13, wherein the polarity of the common voltage, with respect to the data voltage supplied to the pixels coupled to the last gate line of said first gate line block, is opposite to that of the common voltage, with respect to the data voltage supplied to the pixels coupled to the first gate line of said second gate line block on the identical pixel column.

Sub C1

15. The LOD of claim 13, wherein the polarity of the common voltage with respect to the data voltage supplied to the pixels coupled to the last gate line of said first gate line block, is identical to that of the common voltage, with respect to the data voltage supplied to the pixels coupled to the first gate line of the second gate line block on the identical pixel column.

Sub B3

16. A method for driving a liquid crystal display (LCD) including a first gate line block having a plurality of first gate lines; a second gate line block formed beneath the first gate line block and having a plurality of second gate lines; a plurality of first data lines crossing and separated from the first gate lines of the first gate line block; and a plurality of second data lines crossing and separated from the second gate lines of the second gate line block, comprising the steps of:

providing sequentially scanning signals to the first gate line of the first gate line block;

providing sequentially scanning signals to the second gate line of the second gate line block in a scanning direction opposite to that of the first gate line block; and

supplying data voltages, which contain image signals, to the first and second data lines so that the data voltages are supplied to the pixels coupled to the gate lines to which the scanning signals are provided.

17. The method of claim 16, wherein the scanning signals are sequentially provided to the first gate line block from the last gate line to the first gate line, and to the second gate line block from the first gate line to the last gate line.

Sub
C1

18. The method of claim 17, wherein the method further comprises the steps of:

writing the image signals to be provided to the first data line to the first frame memory;

5 writing the image signals to be provided to the second data line to the second frame memory;

outputting the image signals to the first data lines in a reverse order as the image signals are written to the first frame memory; and

10 outputting the image signals to the second data lines in the same order as the image signals are written to the second frame memory.

Sub
B6

19. The method of claim 16, wherein the scanning signals are sequentially provided to the first gate line block from the first gate line to the last gate line, and to the second gate line block from the last gate line to the first gate line.

Sub
C4

20. The method of claim 19, wherein the method further comprises the steps of:

writing the image signals to be provided to the first data line to the first frame memory;

20 writing the image signals to be provided to the second data line to the second frame memory;

outputting the image signals to the first data lines in the same order as the image signals are written to the first frame memory; and

outputting the image signals to the second data lines in a reverse opposite order as the image signals are written to the second frame memory.

add B7